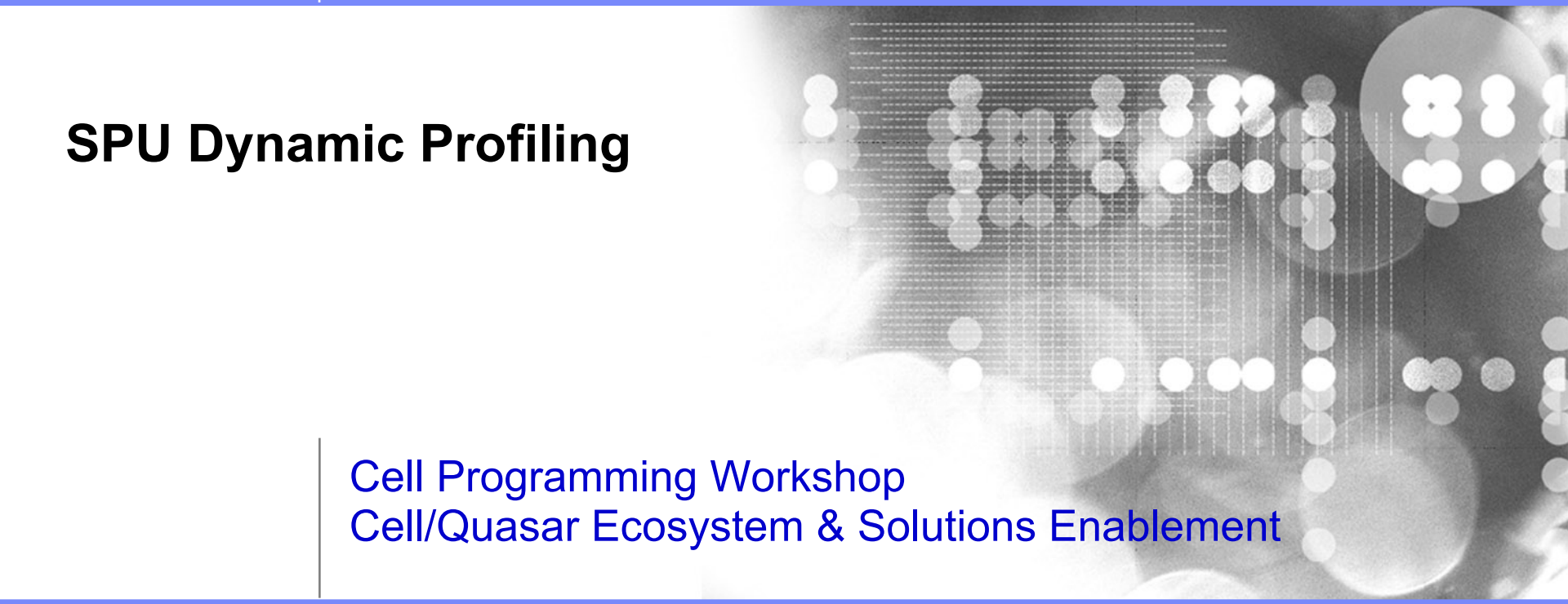


SPU Dynamic Profiling

Cell Programming Workshop
Cell/Quasar Ecosystem & Solutions Enablement

Course Objectives

- To familiarize with the SPU dynamic profiling capability provided by the IBM full system simulator

Course Agenda

- SPU performance model
- SPU pipeline statistics
- SPE visualizer
- Local Store stats

SPU Dynamic Performance Profile Checkpoints

```
#include "profile.h"
```

C header to enable profiling

```
prof_clear();    // clear performance info
prof_start();  // start recording performance info

< something interesting >

prof_stop();  // stop recording performance info
```

Generates `SPU0: CP31, 83(82), 4565`

SPU #

Checkpoint #

Instruction counter Total (excl. no-op)

Cycle counter

SPU Performance Model

- **Referred to in the simulator as “pipeline mode”**
- **Models salient SPU microarchitectural behavior**
  - In-order issue
  - No register renaming
  - Software-controlled branch hints (no HW predict)
  - LS arbitration rules
  - Destructive ILB prefetch load
  - Instruction run-out

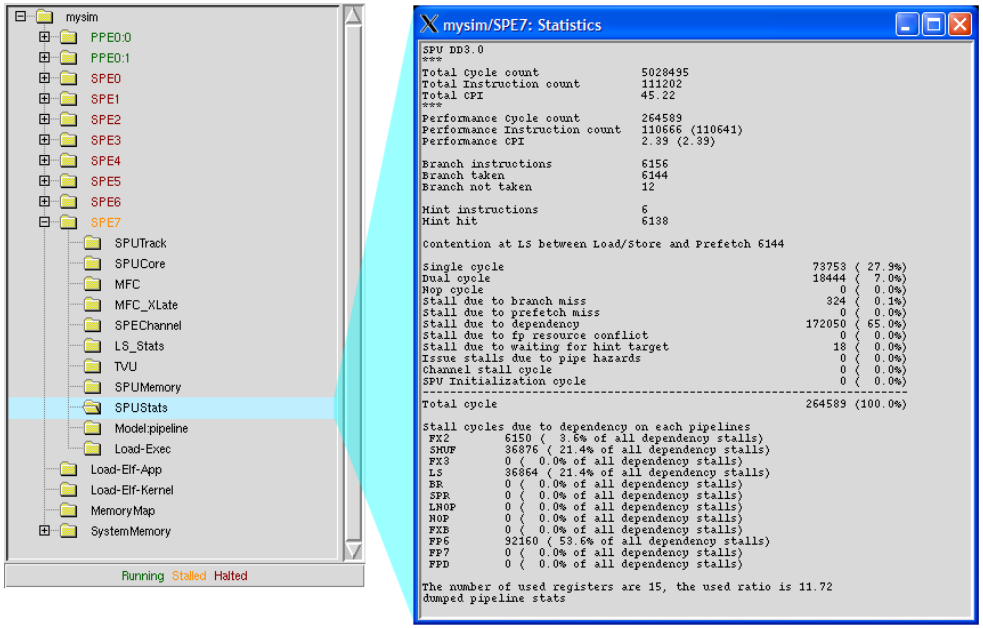
SPU Instruction Mappings by Class

Inst Class	*Exec Pipe*	*Exec Cycles*	*Issue Stall Cycles*	*Instruction Types*
BR	odd (1)	4	0	Branch
FP6	even (0)	6	0	Single precision floating point
FP7	even (0)	7	0	Integer multiply, integer/float conversion, interpolate
FPD	even (0)	7	6	Double precision floating point
FX2	even (0)	2	0	Load immediate, logical operations, integer add/subtract, sign extend, count leading zeros, select bits, carry/borrow generate
FX3	even (0)	4	0	Element rotate/shift
FXB	even (0)	4	0	Special byte operations
LNOP	odd (1)	0	0	No-op
LS	odd (1)	6	0	Loads/stores, branch hints
NOP	even (0)	0	0	No-op
SHUF	odd (1)	4	0	Shuffle bytes, quadword rotate/shift, estimate, gather, form select mask, generate insertion control
SPR	odd (1)	6	0	Channel operations, move to/from SPR

Obtaining SPU Pipeline Statistics

- **Via TCL Commands**
  - `$sim spu n stats print`
  - `array set s [$sim spu n stats export]`
  - `$sim spu n display statistics …`

- **Via GUI Controls**



SPU Stats Summary: `mysim spu n stats print`

```
SPU DD3.0
***
Total Cycle count                 22082564
Total Instruction count           2583628
Total CPI                         8.55
***
Performance Cycle count           6153081
Performance Instruction count     2573522 (2572961)
Performance CPI                   2.39 (2.39)

Branch instructions               143160
Branch taken                      142880
Branch not taken                  280

Hint instructions                 140
Hint hit                          142740

Contention at LS between Load/Store and Prefetch 142880

Single cycle                                          1715121 ( 27.9%)
Dual cycle                                             428920 (  7.0%)
Nop cycle                                                   0 (  0.0%)
Stall due to branch miss                                 7560 (  0.1%)
Stall due to prefetch miss                                  0 (  0.0%)
Stall due to dependency                               4001060 ( 65.0%)
Stall due to fp resource conflict                           0 (  0.0%)
Stall due to waiting for hint target                      420 (  0.0%)
Issue stalls due to pipe hazards                            0 (  0.0%)
Channel stall cycle                                         0 (  0.0%)
SPU Initialization cycle                                    0 (  0.0%)
-------------------------------------------------------------------------
Total cycle                                           6153081 (100.0%)

Stall cycles due to dependency on each pipelines
 FX2        143020 (  3.6% of all dependency stalls)
 SHUF       857560 ( 21.4% of all dependency stalls)
 FX3        0 (  0.0% of all dependency stalls)
 LS         857280 ( 21.4% of all dependency stalls)
 BR         0 (  0.0% of all dependency stalls)
 SPR        0 (  0.0% of all dependency stalls)
 LNOP       0 (  0.0% of all dependency stalls)
 NOP        0 (  0.0% of all dependency stalls)
 FXB        0 (  0.0% of all dependency stalls)
 FP6        2143200 ( 53.6% of all dependency stalls)
 FP7        0 (  0.0% of all dependency stalls)
 FPD        0 (  0.0% of all dependency stalls)

The number of used registers are 15, the used ratio is 11.72
```

Stats totaled for entire execution of SPU, unaffected by **`prof_CP*()`**

Stats totaled in regions bracketed by **`prof_CP30()`** and **`prof_CP31()`**

mysim/SPE7: Statistics

```
SPU DD3.0
***
Total Cycle count                 478434
Total Instruction count           133990
Total CPI                         3.57
***
Performance Cycle count           378304
Performance Instruction count     131456 (131264)
Performance CPI                   2.88 (2.88)

Branch instructions               16384
Branch taken                      16320
Branch not taken                  64

Hint instructions                 64
Pipeline flushes                  64
SP operations (MADDs=2)           0
DP operations (MADDs=2)           65536

Contention at LS between Load/Store and Prefetch 16384

Single cycle                                          98368 ( 26.0%)
Dual cycle                                            16448 (  4.3%)
Nop cycle                                                 0 (  0.0%)
Stall due to branch miss                               1152 (  0.3%)
Stall due to prefetch miss                                0 (  0.0%)
Stall due to dependency                              163904 ( 43.3%)
Stall due to fp resource conflict                         0 (  0.0%)
Stall due to waiting for hint target                    128 (  0.0%)
Issue stalls due to pipe hazards                      98304 ( 26.0%)
Channel stall cycle                                       0 (  0.0%)
SPU Initialization cycle                                  0 (  0.0%)
-------------------------------------------------------------------------
Total cycle                                          378304 (100.0%)

Stall cycles due to dependency on each instruction class
 FX2        64 (  0.0% of all dependency stalls)
 SHUF       0 (  0.0% of all dependency stalls)
 FX3        0 (  0.0% of all dependency stalls)
 LS         65536 ( 40.0% of all dependency stalls)
 BR         0 (  0.0% of all dependency stalls)
 SPR        0 (  0.0% of all dependency stalls)
 LNOP       0 (  0.0% of all dependency stalls)
 NOP        0 (  0.0% of all dependency stalls)
 FXB        0 (  0.0% of all dependency stalls)
 FP6        0 (  0.0% of all dependency stalls)
 FP7        0 (  0.0% of all dependency stalls)
 FPD        98304 ( 60.0% of all dependency stalls)

The number of used registers are 8, the used ratio is  6.25

Instruction Class                                 Insts Issued    Insts Exec    Exec Cycles    Cycles/Inst
-----------------------------------------------   ------------    ----------    -----------    -----------
FX2 (EVEN): Logical and integer arithmetic               49344         49344          82304           1.67
SHUF (ODD): Shuffle, quad rotate/shift, mask                 0             0              0           0.00
FX3 (EVEN): Element rotate/shift                             0             0              0           0.00
LS    (ODD): Load/store, hint                            49152         49216         163968           3.33
BR    (ODD): Branch                                      16384         16384          65536           4.00
SPR   (ODD): Channel and SPR moves                         192             0            640           0.00
LNOP (ODD): NOP                                             64           128              0           0.00
NOP (EVEN): NOP                                              0             0              0           0.00
FXB (EVEN): Special byte ops                                 0             0              0           0.00
FP6 (EVEN): SP floating point                                0             0              0           0.00
FP7 (EVEN): Integer mult, float conversion                   0             0              0           0.00
FPD (EVEN): DP floating point                            16384         16384         114688           7.00

dumped pipeline stats
```

New in SDK 3.0

Pipeline stats

Cycle and Instruction Counts

```
SPU DD3.0
***
Total Cycle count                22082564
Total Instruction count          2583628
Total CPI                        8.55
***
Performance Cycle count          6153081
Performance Instruction count    2573522  (2572961)
Performance CPI                  2.39  (2.39)

Branch instructions              143160
Branch taken                     142880
Branch not taken                 280

Hint instructions                140
Hint hit                         142740

Contention at LS between Load/Store and Prefetch 142880
```

Total Cycle Count: Total SPU run cycles

Total Instruction Count: Total SPU instructions executed

Performance Cycle Count: Total cycles within `prof_CP30/31` brackets

Performance NOP Count: Total NOP instructions executed within `prof_CP30/31` brackets

Performance Instruction Count: Total instructions executed within `prof_CP30/31` brackets

Branch and Hint Stats

```
SPU DD3.0
***
Total Cycle count                 22082564
Total Instruction count           2583628
Total CPI                         8.55
***
Performance Cycle count           6153081
Performance Instruction count     2573522 (2572961)
Performance CPI                   2.39 (2.39)

Branch instructions               143160
Branch taken                      142880
Branch not taken                  280

Hint instructions                 140
Hint hit                          142740

Contention at LS between Load/Store and Prefetch 142880
```

Branch Instructions: Total branch-type instructions executed (excl. stop, sync's, iret)

Branch Taken: Total "satisfied" branches (regardless of PC address change)

Branch Not Taken: (Branch instructions – Branch Taken

Hint Instructions: Count of HBR-type instructions executed (excl. hbrp)

Hint Hits: Count of executed instructions which were loaded from the hint target prefetch buffer

LS Contention: Count of cycles in which LS arbitration prevented instruction prefetch in favor of register load/store operations

Efficiency Stats

```
Single cycle                                          1715121 ( 27.9%)
Dual cycle                                             428920 (  7.0%)
Nop cycle                                                   0 (  0.0%)
Stall due to branch miss                                 7560 (  0.1%)
Stall due to prefetch miss                                  0 (  0.0%)
Stall due to dependency                               4001060 ( 65.0%)
Stall due to fp resource conflict                           0 (  0.0%)
Stall due to waiting for hint target                      420 (  0.0%)
Issue stalls due to pipe hazards                            0 (  0.0%)
Channel stall cycle                                         0 (  0.0%)
SPU Initialization cycle                                    0 (  0.0%)
-------------------------------------------------------------------------
Total cycle                                           6153081 (100.0%)

Stall cycles due to dependency on each pipelines
 FX2         143020 (  3.6% of all dependency stalls)
 SHUF        857560 ( 21.4% of all dependency stalls)
 FX3              0 (  0.0% of all dependency stalls)
 LS          857280 ( 21.4% of all dependency stalls)
 BR               0 (  0.0% of all dependency stalls)
 SPR              0 (  0.0% of all dependency stalls)
 LNOP             0 (  0.0% of all dependency stalls)
 NOP              0 (  0.0% of all dependency stalls)
 FXB              0 (  0.0% of all dependency stalls)
 FP6        2143200 ( 53.6% of all dependency stalls)
 FP7              0 (  0.0% of all dependency stalls)
 FPD              0 (  0.0% of all dependency stalls)

The number of used registers are 15, the used ratio is 11.72
```

Single Cycle: Cycles in which only 1 non-NOP instruction was executed

Dual Cycle: Cycles in which 2 non-NOP instructions were executed

NOP Cycle: Cycles in which only NOP instructions were executed

Branch Miss Stalls: Cycles in which branch mispredict prevented any instruction from executing

Prefetch Miss Stalls: Cycles in which instruction run-out occurred

Dependency Stalls: Cycles in which source/target operand dependencies prevented any instruction from being issued

FP Resource Stalls: Cycles in which shared use of FPU stages prevented any instruction from being issued (e.g. FXB, FP6, FP7, FPD)

Dependency Statistics

```
Single cycle                                          1715121 ( 27.9%)
Dual cycle                                             428920 (  7.0%)
Nop cycle                                                   0 (  0.0%)
Stall due to branch miss                                 7560 (  0.1%)
Stall due to prefetch miss                                  0 (  0.0%)
Stall due to dependency                                4001060 ( 65.0%)
Stall due to fp resource conflict                           0 (  0.0%)
Stall due to waiting for hint target                      420 (  0.0%)
Issue stalls due to pipe hazards                            0 (  0.0%)
Channel stall cycle                                         0 (  0.0%)
SPU Initialization cycle                                    0 (  0.0%)
-------------------------------------------------------------------------
Total cycle                                            6153081 (100.0%)

Stall cycles due to dependency on each pipelines
 FX2         143020 (  3.6% of all dependency stalls)
 SHUF        857560 ( 21.4% of all dependency stalls)
 FX3              0 (  0.0% of all dependency stalls)
 LS          857280 ( 21.4% of all dependency stalls)
 BR               0 (  0.0% of all dependency stalls)
 SPR              0 (  0.0% of all dependency stalls)
 LNOP             0 (  0.0% of all dependency stalls)
 NOP              0 (  0.0% of all dependency stalls)
 FXB              0 (  0.0% of all dependency stalls)
 FP6        2143200 ( 53.6% of all dependency stalls)
 FP7              0 (  0.0% of all dependency stalls)
 FPD              0 (  0.0% of all dependency stalls)

The number of used registers are 15, the used ratio is 11.72
```

Hint Target Stall: Cycles for which target load delay for a hinted branch prevented instruction fetch

Pipe Hazard Stall: Cycles for which pipeline scheduling hazards prevented instruction issue

Channel Stall: Cycles for which the pipeline was stalled waiting on channel operations to complete

Init Cycles: Cycles elapsed in SPU pipeline initialization sequence

Dependency Breakdown: Operand dependency stall cycles by instruction class

Register Utilization: Number of SPU registers read or written

Instruction Histogram: `mysim spu n display statistics hist`

mnemonic	
lnop	281
hbra	140
a	142880
and	141
ai	428640
brz	143020
stqx	285760
lqa	142880
br	140
fsmbi	140
lqx	571520
rotqby	142880
nop	140
il	280
ila	140
cgti	140
fm	142880
ceq	142880
shufb	142880
fma	285760

Branch History: `mysim spu n display statistics branch`

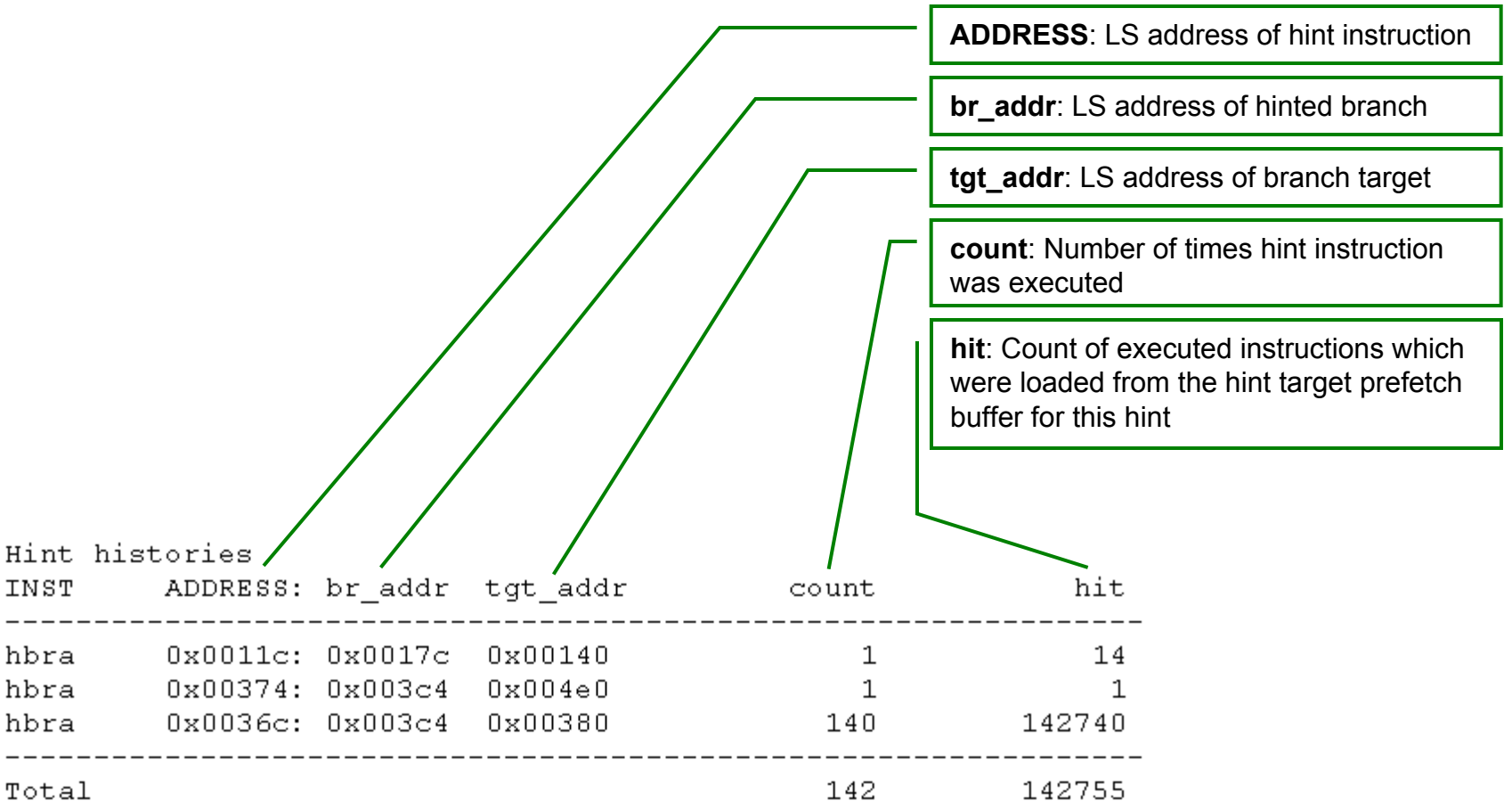
Hit: Count of executed instructions which were loaded from the hint target prefetch buffer for this branch

Hint: Number of executed hint instructions referencing this branch

Branch histories

INST	ADDRESS:	count	taken	not_taken	hint	hit
brsl	0x00014:	1	1	0	0	0
brnz	0x0017c:	15	14	1	1	14
brnz	0x001c4:	1	0	1	0	0
brnz	0x0026c:	1	0	1	0	0
bi	0x00274:	1	1	0	0	0
br	0x003c4:	142881	142741	140	141	142741
sync	0x004e0:	1	0	1	0	0
bi	0x004ec:	1	1	0	0	0
brnz	0x0004c:	28	27	1	0	0
stop	0x00090:	1	0	1	0	0
br	0x0009c:	32	32	0	0	0
bi	0x3fe14:	1	1	0	0	0
brnz	0x000d4:	1	1	0	0	0
brsl	0x000fc:	1	1	0	0	0
brz	0x00364:	140	0	140	0	0
br	0x003cc:	140	140	0	0	0
Total		143246	142960	286	142	142755

Hint History: `mysim spu n display statistics hint`

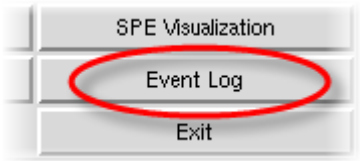


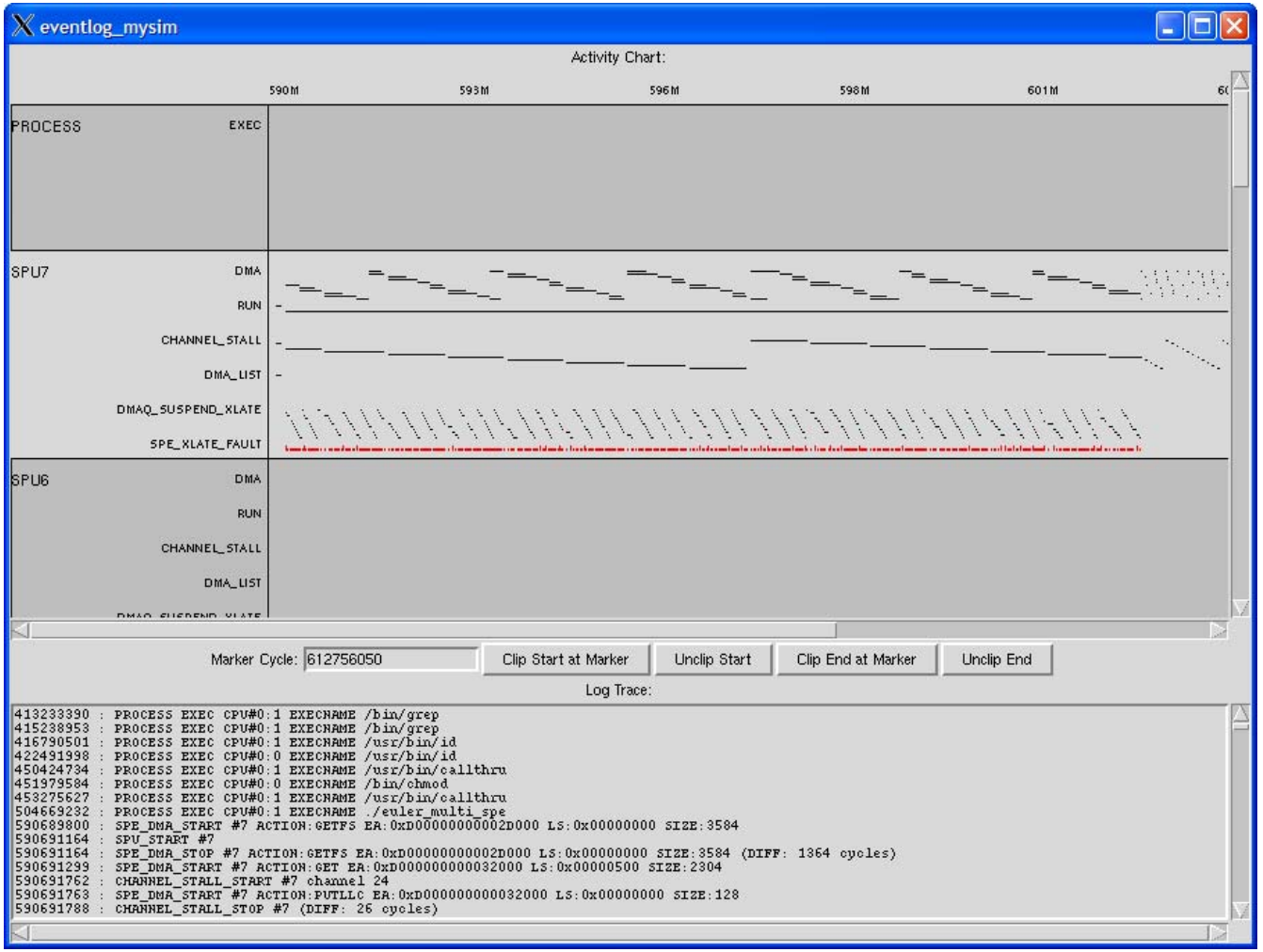

```
Hint histories
INST      ADDRESS: br_addr  tgt_addr          count             hit
-------------------------------------------------------------------
hbra      0x0011c: 0x0017c  0x00140               1              14
hbra      0x00374: 0x003c4  0x004e0               1               1
hbra      0x0036c: 0x003c4  0x00380             140          142740
-------------------------------------------------------------------
Total                                           142          142755
```

Register Utilization: `mysim spu n display statistics reguse`

Register use:	READS(%tot)	WRITES(%tot)	R+W(%tot)
2:	1000300(14.00)	857420(12.00)	1857720(26.00)
3:	428640(6.00)	428640(6.00)	857280(12.00)
4:	142880(2.00)	142880(2.00)	285760(4.00)
5:	142880(2.00)	142880(2.00)	285760(4.00)
6:	142880(2.00)	142880(2.00)	285760(4.00)
7:	857280(12.00)	143020(2.00)	1000300(14.00)
8:	428640(6.00)	143020(2.00)	571660(8.00)
9:	143020(2.00)	0(0.00)	143020(2.00)
10:	285760(4.00)	143020(2.00)	428780(6.00)
12:	428640(6.00)	0(0.00)	428640(6.00)
13:	142880(2.00)	140(0.00)	143020(2.00)
14:	285760(4.00)	0(0.00)	285760(4.00)
16:	285760(4.00)	0(0.00)	285760(4.00)
17:	285760(4.00)	0(0.00)	285760(4.00)
31:	282(0.00)	141(0.00)	423(0.01)
TOTAL use:	5001362(69.99)	2144041(30.01)	7145403

Event Log Sample





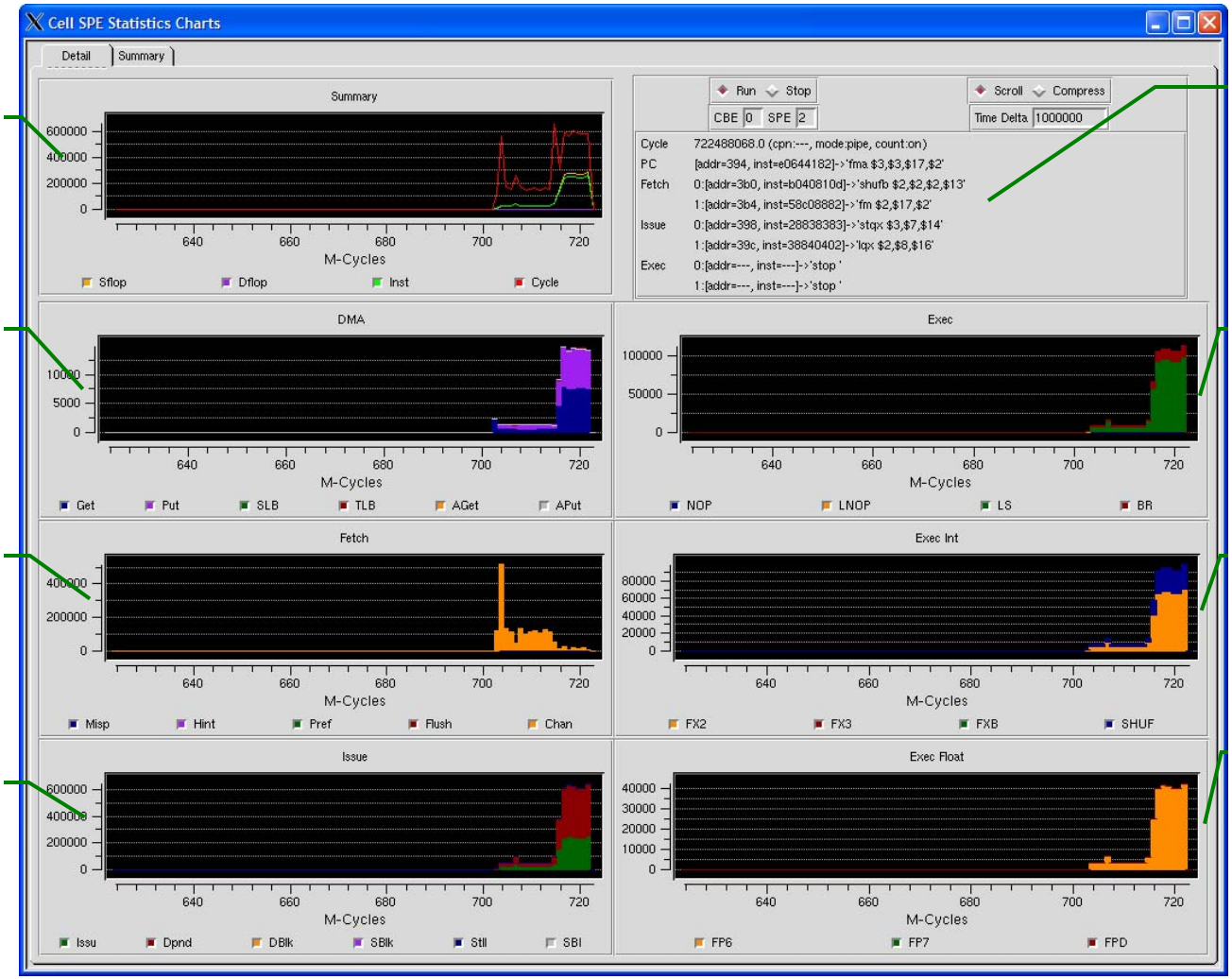
SPE Visualizer Detail Display

Summary: Cycle/Inst counts, SP/DP FLOP

DMA Op Counts: Gets, Puts, Translation Faults, Atomic get/put

Fetch Group: Mispredict, Hint/Prefetch/Channel stalls, Flush count

Issue Group: Issue count, Oper/Hazard stalls, DP/SP block, SBI contention



Control Panel: Pause/Resume, Focal BE/SPU, Scroll/Compress mode, Sampling delta

General Exec: NOP, Load/Store, Branch counts

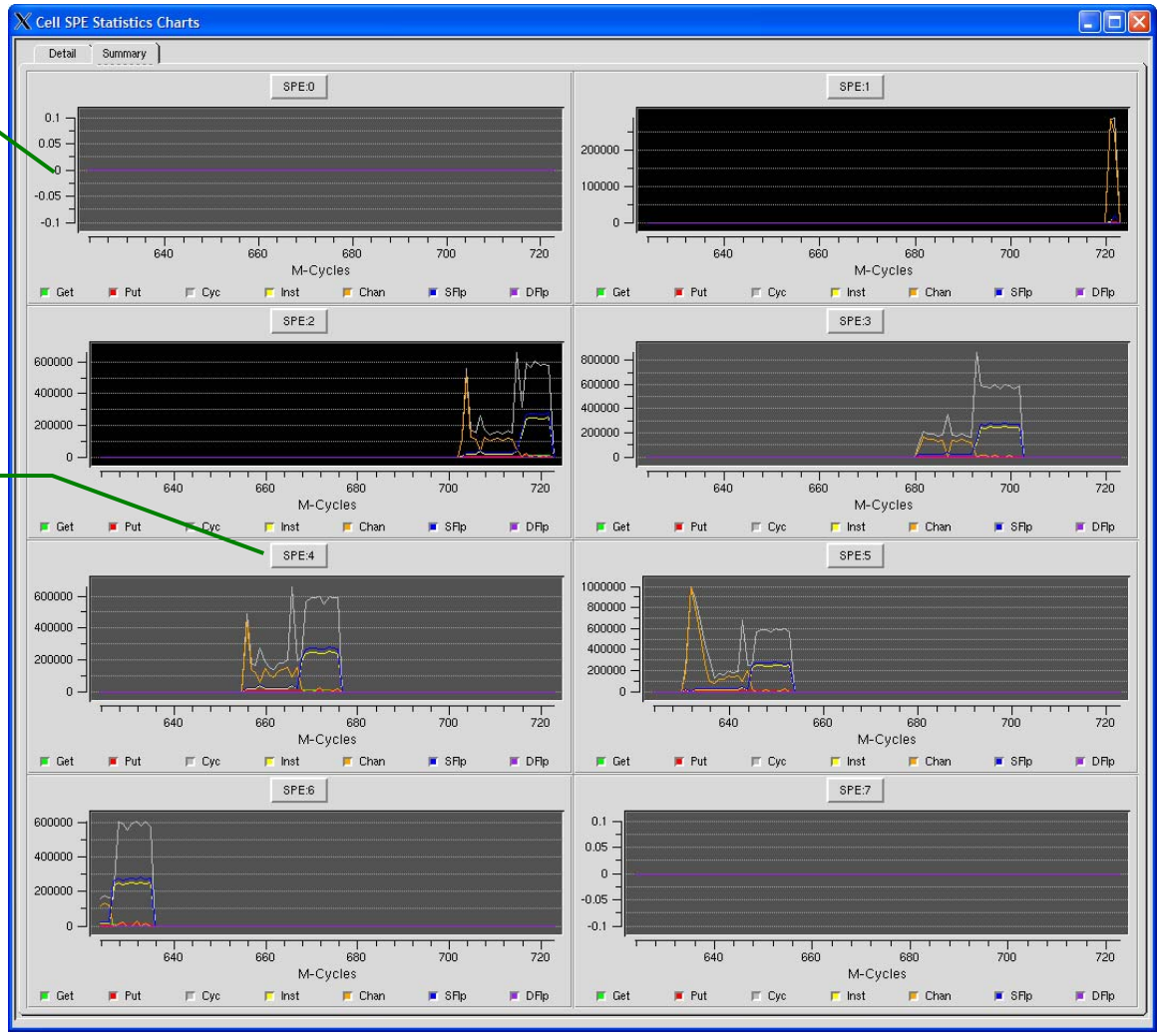
Integer Exec: 2 and 3 cycle FX, Bit op, Shuffle counts

Float Exec: 6 and 7 cycle SP, DP counts

SPU Visualizer Summary Display

Summary: DMA Put/Get, Cycle/Inst counts, Chan stalls, SP/DP FLOP

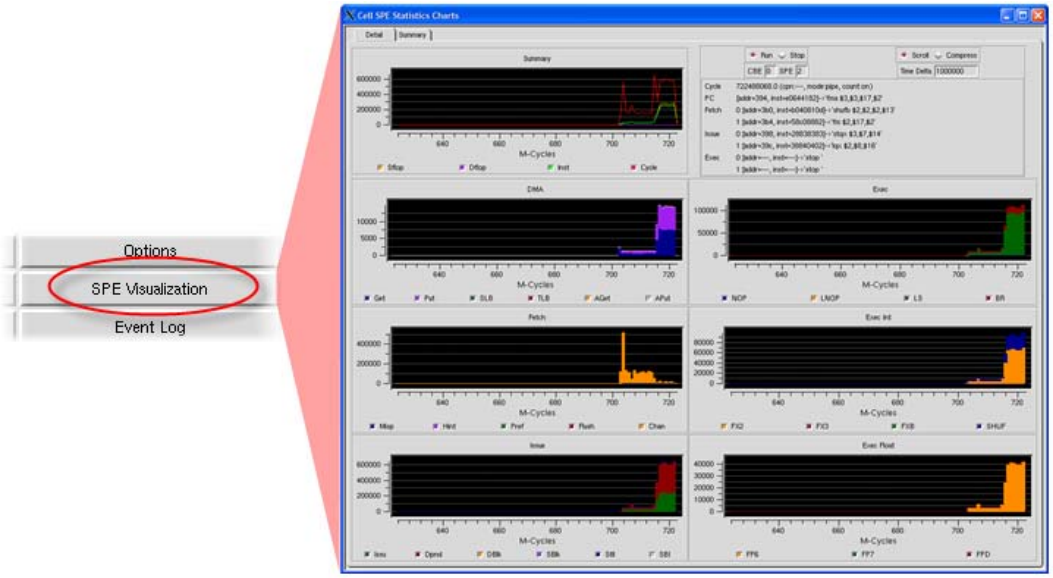
SPE Detail Shortcut



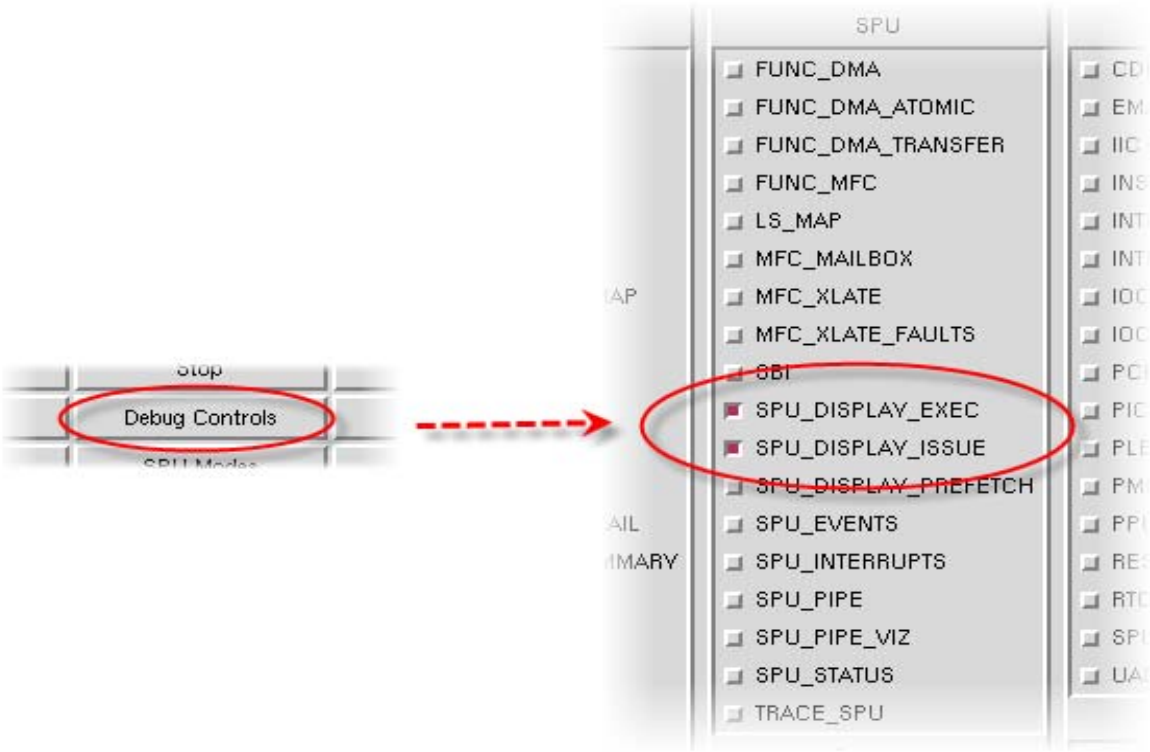
SPE Visualizer Controls

- **Via TCL Commands**
  - `mysim pviz run/stop`
  - `mysim pviz set spu n`
  - `mysim pviz set delta x`
  - `mysim pviz set scroll/compress`
- **Via "apu_callthru.h"**
  - `MamboPVIZRun()`
  - `MamboPVIZStop()`
  - `MamboPVIZSetDelta(x)`

- **Via GUI Controls**



Enabling SPU Pipe Trace

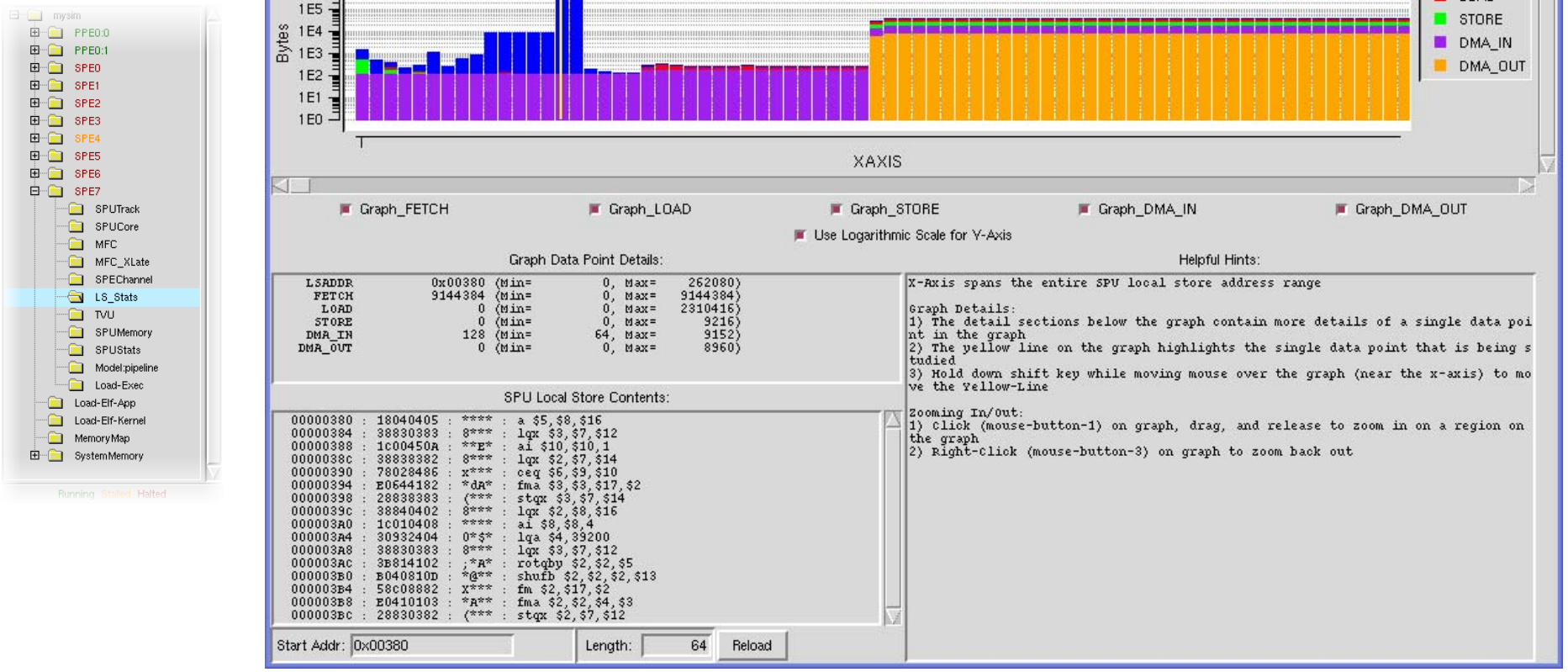


Pipe Trace Output

```
CYCLE: 605035779, SPU-7 CYCLE: 14373254 (Inst: 683872)
mispred 0 -> 003a8
hint 003c4->00380*
pre-fetch ------- ------- 2-00480 1-00400 pre-fetch ls ------- ------- ------- ------- ------- -------
ilbh1 = 00380, ilbh2 = 003c0
ilb11 X 00000, ilb12 X 00000, ilb21 X 00000, ilb22 X 00000
pred = 00380 (8)
 g   = 0x00380 a $5,$8,$16              = 0x00384 lqx $3,$7,$12
 h   = 0x003c0 ai $7,$7,16              = 0x003c4 brz $6,.-68
 i   = 0x003b8 fma $2,$2,$4,$3          = 0x003bc stqx $2,$7,$12
 j   = 0x003b0 shufb $2,$2,$2,$13       = 0x003b4 fm $2,$17,$2
*    X 0x00000 stop                     = 0x003ac rotqby $2,$2,$5      ( -1) (  2)
k    X 0x00000 stop                     R 0x00000 stop                 ( -1) ( -1)
l    X 0x00000 stop                     R 0x00000 stop                 ( -1) ( -1)
m    X 0x00000 stop                     R 0x00000 stop                 ( -1) ( -1)
n    X 0x00000 stop                     = 0x003a8 lqx $3,$7,$12        ( -1) (  3)
o    = 0x003a0 ai $8,$8,4               = 0x003a4 lqa $4,39200         (128) (  4)
p    X 0x00000 stop                     = 0x0039c lqx $2,$8,$16        ( -1) (128)
q    X 0x00000 stop                     = 0x00398 stqx $3,$7,$14       ( -1) (128)
r    R 0x00000 stop                     X 0x00000 stop                 ( -1) ( -1)
s    R 0x00000 stop                     X 0x00000 stop                 ( -1) ( -1)
t    R 0x00000 stop                     X 0x00000 stop                 ( -1) ( -1)
u    R 0x00000 stop                     X 0x00000 stop                 ( -1) ( -1)
v    R 0x00000 stop                     X 0x00000 stop                 ( -1) ( -1)
CYCLE: 605035780, SPU-7 CYCLE: 14373255 (Inst: 683873)
mispred 0 -> 003ac
hint 003c4->00380*
pre-f                                                                              -------
ilbh1
ilb11
pred = 00380 (8)
 g   = 0x00380 a $5,$8,$16              = 0x00384 lqx $3,$7,$12
 h   = 0x003c0 ai $7,$7,16              = 0x003c4 brz $6,.-68
 i   = 0x003b8 fma $2,$2,$4,$3          = 0x003bc stqx $2,$7,$12
 j   = 0x003b0 shufb $2,$2,$2,$13       = 0x003b4 fm $2,$17,$2
*    R 0x00000 stop                     X 0x00000 stop                 ( -1) ( -1)
k    X 0x00000 stop                     = 0x003ac rotqby $2,$2,$5      ( -1) (  2)
```

http://www-128.ibm.com/developerworks/power/library/pa-cellspu/

Local Store Stats



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