

IBM Systems & Technology Group Cell/Quasar Ecosystem & Solutions Enablement

SPU Dynamic Profiling

Cell Programming Workshop Cell/Quasar Ecosystem & Solutions Enablement

Cell Programming Workshop

Course Objectives

 To familiarize with the SPU dynamic profiling capability provided by the IBM full system simulator

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Course Agenda

- SPU performance model
- SPU pipeline statistics
- SPE visualizer
- Local Store stats

SPU Dynamic Performance Profile Checkpoints

```
#include "profile.h"
```

```
C header to enable profiling
prof_clear(); // clear performance info
prof_start(); // start recording performance info
```

< something interesting >

prof stop(); // stop recording performance info



SPU Performance Model

- Referred to in the simulator as "pipeline mode"
- Models salient SPU microarchitectural behavior
 - In-order issue
 - No register renaming
 - Software-controlled branch hints (no HW predict)
 - LS arbitration rules
 - Destructive ILB prefetch load
 - Instruction run-out



SPU Instruction Mappings by Class

Inst Class	Exec Pipe	Exec Cycles	lssue Stall Cycles	Instruction Types
BR	odd (1)	4	0	Branch
FP6	even (0)	6	0	Single precision floating point
FP7	even (0)	7	0	Integer multiply, integer/float conversion, interpolate
FPD	even (0)	7	6	Double precision floating point
FX2	even (0)	2	0	Load immediate, logical operations, integer add/subtract, sign extend, count leading zeros, select bits, carry/borrow generate
FX3	even (0)	4	0	Element rotate/shift
FXB	even (0)	4	0	Special byte operations
LNOP	odd (1)	0	0	No-op
LS	odd (1)	6	0	Loads/stores, branch hints
NOP	even (0)	0	0	No-op
SHUF	odd (1)	4	0	Shuffle bytes, quadword rotate/shift, estimate, gather, form select mask, generate insertion control
SPR	odd (1)	6	0	Channel operations, move to/from SPR

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Obtaining SPU Pipeline Statistics

Via TCL Commands

- \$sim spu n stats print
- array set s [\$sim spu n stats export]
- \$sim spu n display statistics ...

Via GUI Controls



TBM

SPU Stats Summary: mysim spu n stats print

The structure count 22002564 Oral Cycle count 22002564 Oral Instruction count 250020 Stats totaled for entire execution SPU, unaffected by prof_CP*(Performance Crit 2.39 (2.39) Performance Crit 2.39 (2.39) Performance Crit 2.39 (2.39) Performance Crit 14360 Performance Crit 1400 Init Instructions 140 Init Instructions 140 Nucl cycle 175511 (27.5%) Wool cycle 0 (0.00) Stats totaled in regions brackete prof_CP30 () and prof_CP3 Stati due to branch miss 0 (0.00) Stall due to preferch miss 0 (0.00) Stall due to prefere miss 0 (0.00) Stall due to dependency 40016 (0.00) Parmel stall cycle 0 (0.00) Stall due to dependency estalls) 0 (0.00)	SPU DD3.0				
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	FPD 0 (0.0% of all de	ependency stalls)			
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The number of used registers are 15, the used ratio is 11.72



	mysim/SPE7: 9	itatistics			_ = ×	ĺ	
SPU DD3.0							
Total Cycle count Total Instruction count Total CPI	478434 133990 3.57						
Performance Cycle count Performance Instruction count Performance CPI	378304 131456 (131264) 2.88 (2.88)					N	lew in SDK 3.0
Branch instructions Branch taken Branch not taken	16384 16320 64						
Hint instructions Pipeline flushes SP operations (MADDs=2) DP operations (MADDs=2)	64 64 0 65536						
Contention at LS between Load/S	Store and Prefetch 16384						
Single cycle Dual cycle Nop cycle Stall due to branch miss Stall due to prefetch miss Stall due to dependency Stall due to fp resource confli Stall due to waiting for hint t Issue stalls due to pipe hazard Channel stall cycle SPU Initialization cycle	ict target ls	98368 16448 0 1152 0 163904 0 128 98304 0 0 0	(26.0%) (4.3%) (0.0%) (0.3%) (2.3%) (2.0%) (2.0%) (2.0%) (2.0%) (2.0%) (0.0%)				
Total cycle		378304	(100.0%)				
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The number of used registers an	re 8, the used ratio is	6.25					
Instruction Class	Insts	Issued	Insts Exec	Exec Cycles	Cycles/Inst		
FN2 (EVEN): Logical and integer SHOF (ODD): Shuffle, quad rotat FN3 (EVEN): Element rotate/shi1 LS (ODD): Load/store, hint ER (ODD): Branch SPR (ODD): Channel and SPR mos LNOP (EVEN): NOP FXE (EVEN): NOP FXE (EVEN): Special byte ops FPE (EVEN): Special byte ops FPE (EVEN): SP floating point FPT (EVEN): DP floating point	r arithmetic te/shift, mask ft zes t conversion	49344 0 49152 16384 192 64 0 0 0 16384	49344 0 49216 16384 128 0 0 0 16384	82304 0 163968 65536 640 0 0 114688	1.67 0.00 3.33 4.00 0.00 0.00 0.00 0.00 0.00		
dumped pipeline stats							



Cycle and Instruction Counts





Branch and Hint Stats

SPU DD3.0 *** Total Cycle count Total Instruction count Total CPI *** Performance Cycle count Performance Instruction count Performance CPI

Branch instructions Branch taken Branch not taken

Hint instructions Hint hit

11

Contention at LS between Load/Store and Prefetch 142880

22082564

2583628

6153081

2573522

143160 142880

280

140

142740

2.39 (2/39

2961

8.55

Branch Instructions: Total branchtype instructions executed (excl. stop, sync's, iret)

Branch Taken: Total "satisfied" branches (regardless of PC address change)

Branch Not Taken: (Branch instructions – Branch Taken

Hint Instructions: Count of HBRtype instructions executed (excl. hbrp)

Hint Hits: Count of executed instructions which were loaded from the hint target prefetch buffer

LS Contention: Count of cycles in which LS arbitration prevented instruction prefetch in favor of register load/store operations

Efficiency Stats

Single cycle	1715121 (27.9%)
Dual cycle	428920 (7.0%)
Nop cycle	0 (0.0%)
Stall due to branch miss	7560 (0.1%)
Stall due to prefetch miss	0 (0.0%)
Stall due to dependency	4001060 (65.0%)
Stall due to fp resource conflict	0 (0.0)
Stall due to waiting for hint target	420 (0.0%)
Issue stalls due to pipe hazards	0 (0.0%)
Channel stall cycle	O (O.O%) 🔪 🔪
SPU Initialization cycle	O (0.0%) 🔪 🔪
	\ \ \ \
Total cycle	6153081 (100.0%)

Stall cycles due to dependency on each pipelines

FX2	143020 (3.6% of all dependency stalls)
SHUF	857560 (21.4% of all dependency stalls)
FX3	0 (0.0% of all dependency stalls)
LS	857280 (21.4% of all dependency stalls)
BR	0 (0.0% of all dependency stalls)
SPR	0 (0.0% of all dependency stalls)
LNOP	0 (0.0% of all dependency stalls)
NOP	0 (0.0% of all dependency stalls)
FXB	0 (0.0% of all dependency stalls)
FP6	2143200 (53.6% of all dependency stalls)
FP7	0 (0.0% of all dependency stalls)
FPD	0 (0.0% of all dependency stalls)

The number of used registers are 15, the used ratio is 11.72

Single Cycle: Cycles in which only 1 non-NOP instruction was executed Dual Cycle: Cycles in which 2 non-NOP instructions were executed

NOP Cycle: Cycles in which only NOP instructions were executed

Branch Miss Stalls: Cycles in which branch mispredict prevented any instruction from executing

Prefetch Miss Stalls: Cycles in which instruction run-out occurred

Dependency Stalls: Cycles in which source/target operand dependencies prevented any instruction from being issued

FP Resource Stalls: Cycles in which shared use of FPU stages prevented any instruction from being issued (e.g. FXB, FP6, FP7, FPD)

Dependency Statistics



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Instruction Histogram: mysim spu n display statistics hist

mnemonic						
+-						
lnop	281					
hbra	140					
а	142880					
and	141					
ai	428640					
brz	143020					
stqx	285760					
lqa	142880					
br	140					
fsmbi	140					
lqx	571520					
rotqby	142880					
nop	140					
il	280					
ila	140					
cgti	140					
fm	142880					
ceq	142880					
shufb	142880					
fma	285760					



Branch History: mysim spu n display statistics branch

			Hit: Cou which w target p	unt of executed vere loaded from refetch buffer fo	instructions the hint or this branch	
Hint: Nur instructio	nber of executed hins referencing this	int branch				
Branch	histories					۱.
INST	ADDRESS:	count	taken	not_taken	hint	hit
brsl	0x00014:	1	1	0	0	0
brnz	0x0017c:	15	14	1	1	14
brnz	0x001c4:	1	0	1	0	0
brnz	0x0026c:	1	0	1	0	0
bi	0x00274:	1	1	0	0	0
br	0x003c4:	142881	142741	(140)	141	142741
sync	0x004e0:	1	0	1	0	0
bi	0x004ec:	1	1	0	0	0
brnz	0x0004c:	28	27	1	0	0
stop	0x00090:	1	0	1	0	0
br	0x0009c:	32	32	0	0	0
bi	Ox3fe14:	1	1	0	0	0
brnz	0x000d4:	1	1	0	0	0
brsl	0x000fc:	1	1	0	0	0
brz	0x00364:	140	0	140	0	0
br	0x003cc:	140	140	0	0	0
Total		143246	142960	286	142	142755



Hint History: mysim spu n display statistics hint





Register Utilization: mysim spu n display statistics reguse

Register use:	READS(%tot)	WRITES(%tot)	R+W(%tot)
2:	1000300(14.00)	857420(12.00)	1857720(26.00)
3:	428640(6.00)	428640(6.00)	857280(12.00)
4:	142880(2.00)	142880(2.00)	285760(4.00)
5:	142880(2.00)	142880(2.00)	285760(4.00)
6:	142880(2.00)	142880(2.00)	285760(4.00)
7:	857280(12.00)	143020(2.00)	1000300(14.00)
8:	428640(6.00)	143020(2.00)	571660(8.00)
9:	143020(2.00)	0(0.00)	143020(2.00)
10:	285760(4.00)	143020(2.00)	428780(6.00)
12:	428640(6.00)	0(0.00)	428640(6.00)
13:	142880(2.00)	140(0.00)	143020(2.00)
14:	285760(4.00)	0(0.00)	285760(4.00)
16:	285760(4.00)	0(0.00)	285760(4.00)
17:	285760(4.00)	0(0.00)	285760(4.00)
31:	282(0.00)	141(0.00)	423(0.01)
TOTAL use:	5001362(69.99)	2144041(30.01)	7145403

3/2/2008



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Event Log Sample

X eventle	og_mysim						
			Activity Cha	art:			
		590M	593 M	596 M	598 M	601M	6(
PROCESS	EXEC						
SPU7	DMA RUN	⁼	- <u>-</u> =		~= [~] =	==, =	
	CHANNEL_STALL						·
	DMA_LIST			<u> </u>			—
	DMAQ_SUSPEND_XLATE						χ
	SPE_XLATE_FAULT	11111111	· · · · · · · · · · · · · · · · · · ·		11.2.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.	ن از از از این از	······
SPU6	DMA RUN CHANNEL_STALL DMA_LIST						
4							
	Marker C	cycle: 612756050	Clip Start at Marker	Unclip Start	Clip End at Marker	Unclip End	
413233390 415238953 416730501 422431398 450424734 450242734 453275627 590663202 590691164 590691164 590691164 590691762 590691762	PROCESS EXEC CPU#0 PROCESS EXEC CPU#0 SPE_DMA_START #7 A SPE_DMA_START #7 A SPE_DMA_START #7 A CHANNEL_STALL_STARD SPE_DMA_START #7 A CHANNEL_STALL_STARD	1 EXECHAME /bin/grep 1 EXECHAME /bin/grep 1 EXECHAME /bin/grep 1 EXECHAME /bir/bin/ 1 EXECHAME /bir/bin/ 1 EXECHAME /bir/chan 1 EXECHAME /bir/chan	Log Trace id id callthru dd callthru nulti_spe 0000000220000 LS:0x0000000 000000320000 LS:0x00000500 0000000320000 LS:0x00000500	: 0 SIZE:3584 1 SIZE:3584 (DIFF SIZE:2304 00 SIZE:128	': 1364 cycles)		ł

SPE Visualizer Detail Display



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SPU Visualizer Summary Display



SPE Visualizer Controls

Via TCL Commands

- mysim pviz run/stop
- mysim pviz set spu n
- mysim pviz set delta x
- mysim pviz set scroll/compress

Via "apu_callthru.h"

- MamboPVIZRun()
- MamboPVIZStop()

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MamboPVIZSetDelta(x)

Via GUI Controls





Enabling SPU Pipe Trace



Pipe Trace Output

1:	: CYCLE: 605035779, SPU-7 CYCLE: 14373254 (Inst: 683872)					
2:	: mispred 0 -> 003a8	,					
3:	hint 003c4->00380*						
4:	pre-fetch 2-00480 1-00400	pre-fetch 1s					
5:	: ilbh1 = 00380, ilbh2 = 003c0	1					
6:	ilb11 x 00000, ilb12 x 00000, ilb21 x 000	00, i1b22 x 00000					
7:	: pred = 00380 (8)						
8:	$q = 0 \times 00380 a \$5, \$8, \$16 =$	0x00384 lqx \$3,\$7,\$12					
9:	: h = 0x003c0 ai \$7,\$7,16 =	0x003c4 brz \$6,68					
10:	: i = 0x003b8 fma \$2,\$2,\$4,\$3 =	0x003bc stqx \$2,\$7,\$12					
11:	: j = 0x003b0 shufb \$2,\$2,\$2,\$13 =	0x003b4 fm \$2,\$17,\$2					
12:	: * X 0x00000 stop =	0x003ac rotqby \$2,\$2,\$5	(-1) (2)				
13:	: k X 0x00000 stop R	0x00000 stop	(-1) (-1)				
14:	: 1 X 0x00000 stop R	0x00000 stop	(-1) (-1)				
15:	:m X 0x00000 stop R	0x00000 stop	(-1) (-1)				
16:	: n X 0x00000 stop =	0x003a8 lqx \$3,\$7,\$12	(-1) (3)				
17:	: o = 0x003a0 ai \$8,\$8,4 =	0x003a4 lqa \$4,39200	(128) (4)				
18:	:p X 0x00000 stop =	0x0039c lqx \$2,\$8,\$16	(-1) (128)				
19:	: q X 0x00000 stop =	0x00398 stqx \$3,\$7,\$14	(-1) (128)				
20:	r R 0x00000 stop X	0x00000 stop	(-1) (-1)				
21:	:s R 0x00000 stop X	0x00000 stop	(-1) (-1)				
22:	:t R 0x00000 stop X	0x00000 stop	(-1) (-1)				
23:	u R 0x00000 stop X	0x00000 stop	(-1) (-1)				
24:	: v R 0x00000 stop X	0x00000 stop	(-1) (-1)				
25:	: CYCLE: 605035780, SPU-7 CYCLE: 14373255 (Inst: 683873)					
26:	: mispred 0 -> 003ac						
27:	: hint 003c4-500300#						
28:	titht http://www-128 ibm com/d	eveloperworks/power/libra	ry/pa-cellspu/				
29:	29: 11bh1 nccp.//www-120.1bm.com/deveroperworks/power/iibrary/pa-celispu/						
30:	30: 11b11						
32.	a = 0x00380 = 55 = 58 = 516 = =	0x00384 lox \$3 \$7 \$12					
33.	h = 0x003c0 ai \$7.\$7.16 =	0x003c4 brz \$6=68					
34:	i = 0x003b8 fma \$2.\$2.\$4.\$3 =	0x003bc stax \$2.\$7.\$12					
35:	i = 0x003b0 shufb \$2,\$2,\$2,\$13 =	0x003b4 fm \$2,\$17,\$2					
36:	: * R 0x00000 stop X	0x00000 stop	(-1) (-1)				
37:	: k X 0x00000 stop	0x003ac rotoby \$2,\$2,\$5	(-1) (2)				

Local Store Stats





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